

Jitter in Clock Sources

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Continuous advances in high-speed communication and measurement systems require higher levels of performance from system clocks and references. Performance acceptable in the past may not be sufficient to support high-speed synchronous equipment. Perhaps the most important and least understood measure of clock performance is jitter.

The purpose of this discussion is fourfold.

1. To define jitter intuitively, and discuss it's properties.
2. To explain how jitter degrades system performance.
3. To describe various practical methods of measuring jitter, including the relevance and ease of each method.
4. Offer guidelines for specifying high-speed clocks and related devices.

Jitter Defined

- **Jitter:** "Short-term variations of the significant instants of a digital signal from their ideal positions in time" (ITU).

The expected edges in a digital datastream never occur exactly where desired. Defining and measuring the timing accuracy of those edges (jitter) is critical to the performance of synchronous communication systems.

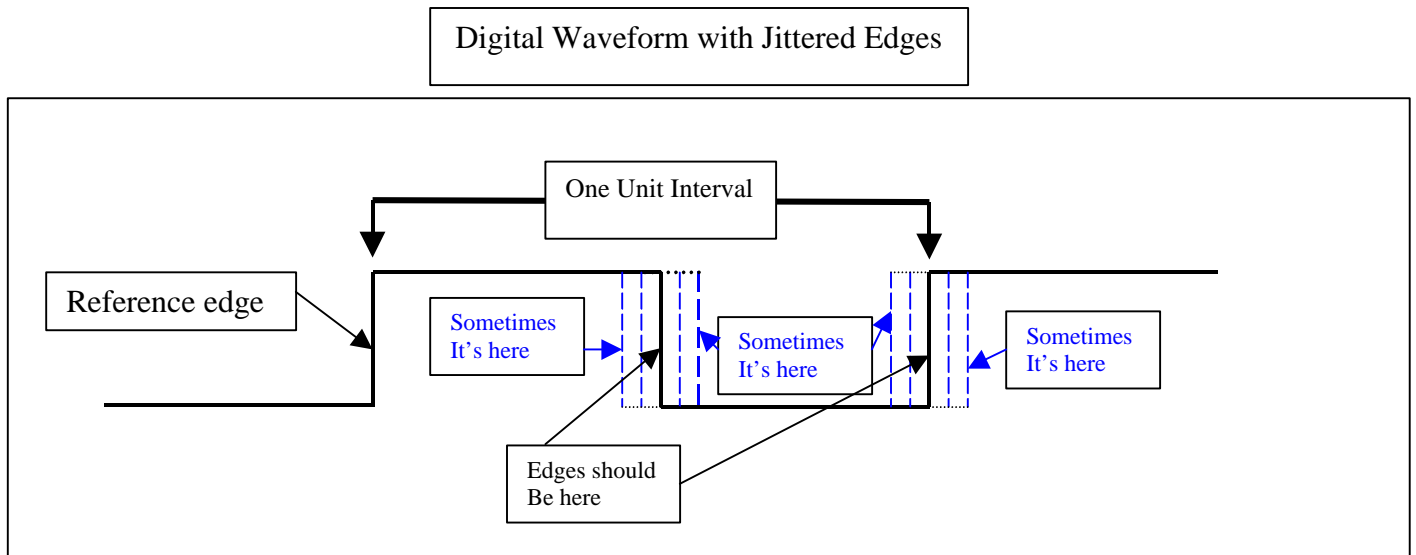


Figure 1

Definition of terms:

- a) Jitter expressed in Unit Intervals: A single unit interval is one cycle of the clock frequency. This is the normalized clock period. Jitter expressed in Unit Intervals describes the magnitude of the jitter as a decimal fraction of one unit interval.
- b) Jitter expressed in degrees (deg.): Jitter expressed in degrees describes the magnitude of the jitter in units of deg. where one cycle equals 360 deg.
- c) Jitter expressed in absolute time: Jitter expressed in units of time describes the magnitude of the jitter in appropriate orders of magnitude, usually picoseconds.
- d) Jitter expressed as a power measurement is described in units of radians or unit intervals squared. Often expressed in dB relative to one cycle-squared (From Bellamy) [1]
- e) Pattern Jitter: Pattern dependent jitter. Sometimes referred to as flanging. Not random in nature. Generally a result of subharmonics. When viewed in the time domain, it is seen as multiple modes of jitter. Pattern jitter is deterministic, it is a phenomenon that may be attributed to a unique source. All other jitter referred to in this discussion is stochastic in nature, and may only be described as a random variable with respect to time.

For example:

Assume a clock rate of 155.52 MHz. One unit interval would be equal to the period of the signal, $1/155.52 \text{ MHz} = 6.43 \text{ nsec.} = 360 \text{ deg.}$

Assume 100 ps Pk-Pk of jitter.

100 Ps of jitter = .01555 unit intervals (UI) of jitter = 5.598 deg. of jitter. (All Pk-Pk)

All three measurements describe the same amount of jitter.

For jitter power, rms (one sigma, σ) measurements are used. For the above case, we approximate Pk-Pk as 7σ , or 7 times the RMS value, placing the rms. jitter power at $.000049 \text{ UI}^2$. $\{(.01555/7)^2\}$. Expressed in dB, relative to one unit interval, jitter power in this case would be $10\log (.000049) = -53.1 \text{ dB}_{\text{ui}}$. As will be seen later, jitter can be derived from power spectral density (phase noise) measurements. Table 1 relates various measures of jitter in a 155.52 MHz system clock

Pk-PkJitter in Seconds	Degrees	Unit interval	Unit Interval	Jitter Power
6.43E-09 = one cycle	Degrees(Pk-Pk)	Pk-Pk UNITS	RMS UNITS	dB _{ui}
	<i>normalized</i>	<i>normalized</i>	<i>normalized</i>	
1.00E-10	5.60	0.015552	0.0022217	-53.07
2.00E-11	1.12	0.003110	0.0004443	-67.05
			<i>(1/7 of Pk-Pk approximation)</i>	

Table 1

Measuring Jitter

Measurement Techniques

Time Domain Measurements

Edge to Edge Jitter Using a Delay Line

A true measure of clock jitter is the accurate position of clock edges over time. The most direct method of examining the placement of edges would be to look at the edges using an oscilloscope. Unfortunately, using standard oscilloscope techniques it is impossible to identify individual clock edges in absolute time. . Any jitter measured with a standard oscilloscope is due to trigger instability. As a result, direct waveform measurements using an oscilloscope (even a very good oscilloscope) are not valid measurements of jitter. An additional technique is used to locate the reference edge, discriminate with time, and examine the jitter on following edges. Figure 3 illustrates this method with a typical configuration.

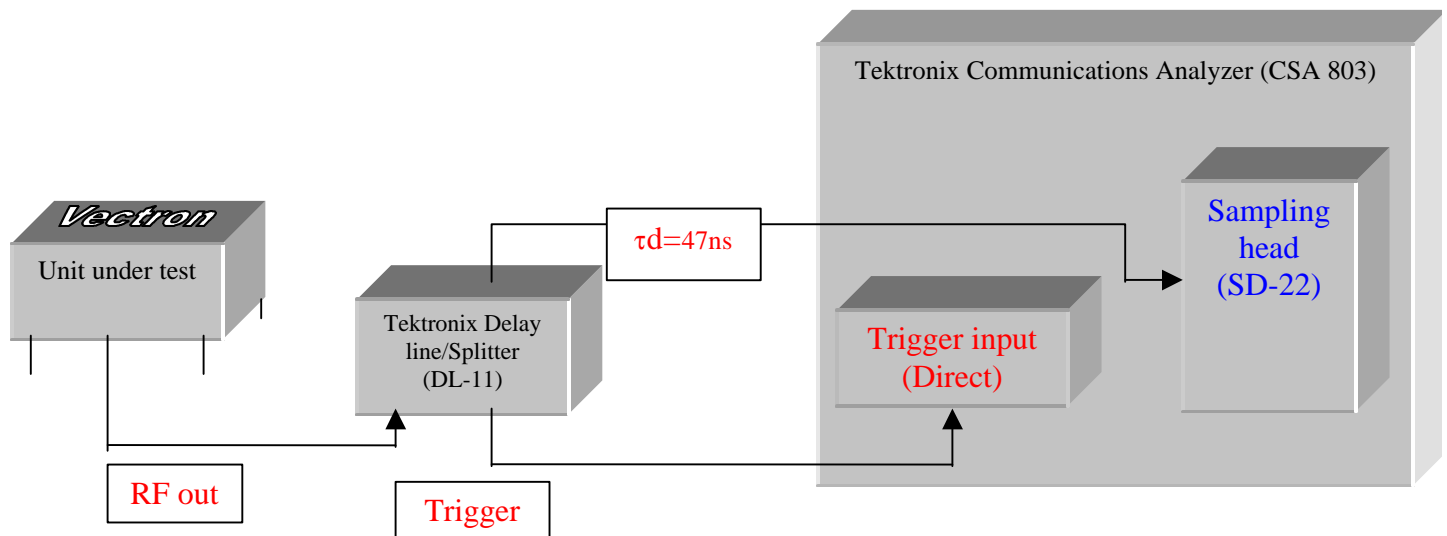
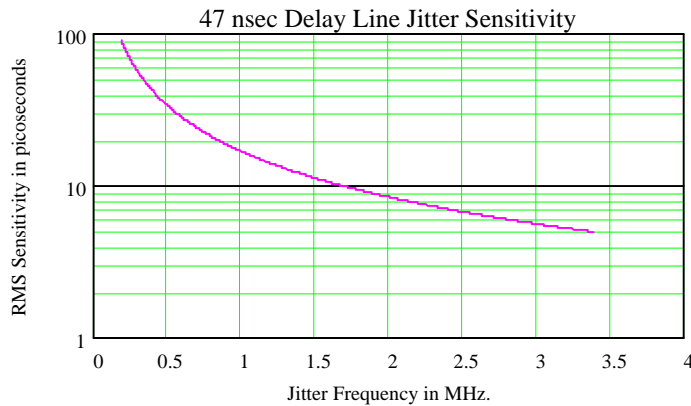


Figure 3

The output of the unit under test is fed into splitter /delay line. The non-delayed output of the splitter is fed to the external trigger input of the oscilloscope (a CSA-803 in this case). The delayed output of the DL-11 is connected to the input of the oscilloscope. By

examining the clock-stream at a time after the trigger equal to the delay used (in this case, 47 nsec), the trigger-edge is located. After the triggered edge has been identified, the next edge is examined. A histogram plot is then produced of the measured jitter of the second edge. A CSA-803 is used for its statistical and histogram capabilities. This is a useful technique limited by the length of the delay line and the speed/sensitivity of the oscilloscope. For all frequencies greater than $1/(2\pi\tau d)$, the measurement is limited by the noise of the oscilloscope. Below $1/(2\pi\tau d)$, the sensitivity drops approximately 20 dB/decade. For the 47-nsec delay shown in fig 3, the corner frequency occurs at 3.3 MHz. All jitter due to frequencies above 3.3 MHz can be resolved to approximately 5 ps using the CSA-803. Jitter at 330 kHz can not be resolved below 50 ps. In a similar manner, jitter at 33 kHz can not be measured below 500 ps. Figure 4 is a plot of RMS jitter sensitivity using a 47-nsec delay line. It is critical to understand the advantages and limitations of this measurement method. For the numerical example given, low frequency jitter below 300 kHz would not be seen. Conversely, jitter due to sidebands 3.0 MHz offset or more could easily be identified. This test method is appropriate when measuring oscillators that employ direct frequency multiplication or where low frequency jitter is not considered. (See previous description of Pattern Jitter).



$$\text{Sens}(f) = 1/2 * \pi * \tau d * f * r$$

Where:

- Sens(f) = jitter sensitivity
- τd = amount of delay used
- f = the jitter frequency to be measured
- r = oscilloscope resolution

Fig. 4

Jitter Measurements Using Phase Locked Loops

It was noted that the length of the delay line limits resolution when measuring edge jitter. In order to measure jitter below 100 Hz offset, one needs merely to order up about three hundred miles of very low loss delay line. In lieu of such a device, phase locked loops are used for a variety of noise measurements.

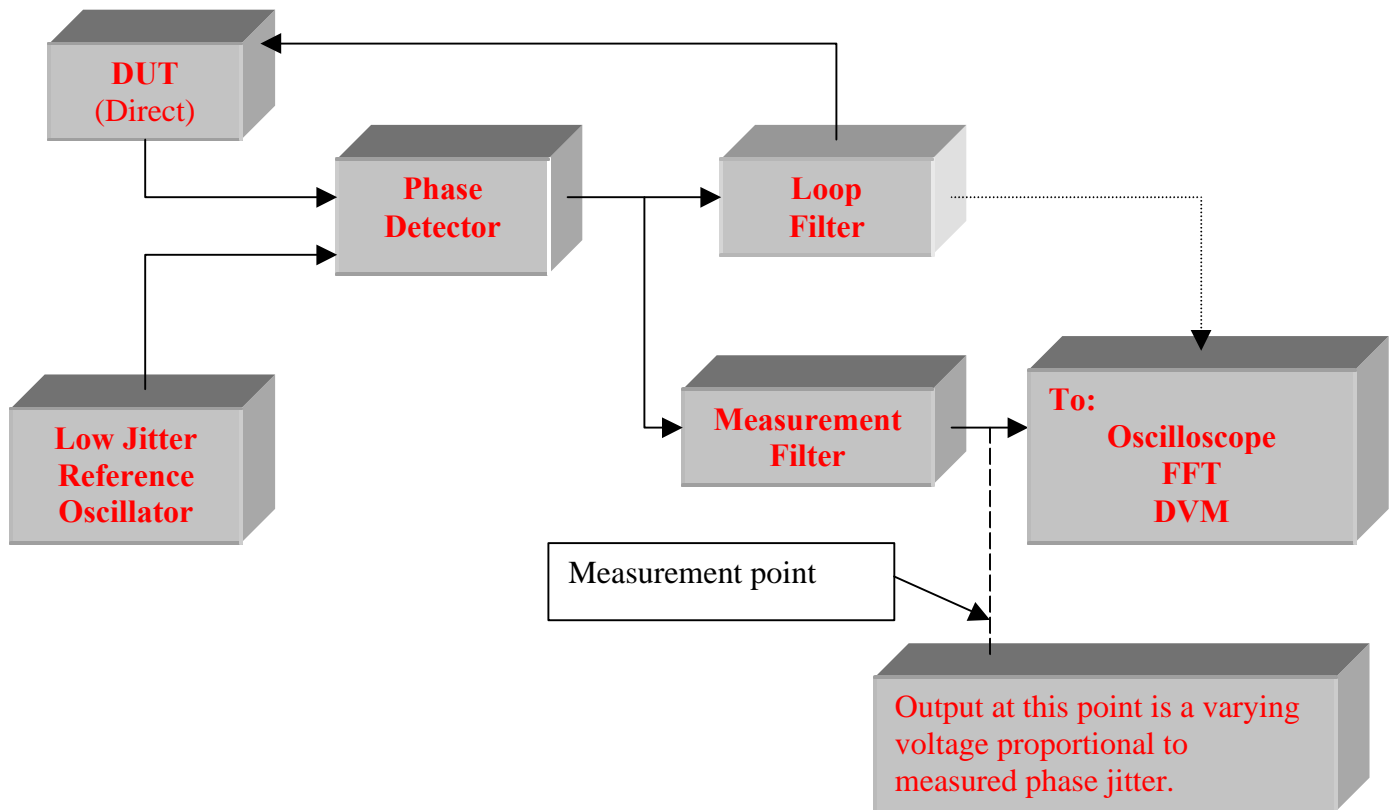


Fig 5

Figure 4 shows the basic elements of a phase locked loop (PLL) used to measure the noise of a clock source. Gardner [5], Best [6], and Woolover [7] are three excellent references for understanding PLLs. Some key loop requirements follow:

- The PLL loop bandwidth is a critical parameter for successful measurements. The system will only measure jitter frequencies outside (higher than) the loop bandwidth. It is recommended that the loop bandwidth be set to a maximum of 1/10 the lowest jitter frequency of interest.
- Loop damping must be set to at least 5 in order to reduce jitter peaking in the PLL. Jitter peaking will increase measured jitter.
- The measurement filter corresponds to jitter bandwidths recommended in Bellcore and ITU specifications. Refer to [2,3] for a list of jitter bandwidths and specifications. Band limiting needs to be defined as a pre-condition for any valid measurement.
- The output of the phase detector (PD) is a varying DC signal that is proportional to the varying phase due to jitter. It is necessary to know the gain constant (K_d) of the PD in volts/radian in order to quantify the detected jitter. For example, a phase detector with a K_d equal to 1 millivolt per degree will

have a peak to peak output of 10 mV for an oscillator with 10 deg. pk-pk jitter. It may be necessary to inject a known amount of jitter in order to calibrate the system for accurate measurements.

Jitter Measurements

Using Phase Locked Loops: Interpreting the Data.

- In The Time Domain

The output signal of the phase detector in Figure 5 contains a wealth of information about the jitter of the measured clock. Direct examination of the signal using an oscilloscope can show Pk-Pk jitter. A true RMS voltmeter can be used to measure RMS (one sigma) jitter. For these measurements, it is critical that the measurement filters used represent the band of jitter frequencies of interest. It would make no sense to measure noise from dc to 10 MHz when a bandwidth of 10 kHz to 1 MHz is required. Oscilloscopes with histogram and statistical capabilities are useful for characterizing the measured jitter.

- In the Frequency Domain

The spectrum of the output signal from the phase detector in Figure 4 represents the spectrum and relative amplitude of jitter in the frequency domain. Examining the spectrum with a low frequency or FFT analyzer gives the most intuitive picture of clock jitter in terms of spectrum. By integrating the signal jitter spectrum over the frequency of interest, it is possible to derive the RMS jitter of the clock. This is the most accurate and unfortunately the most cumbersome method for characterizing jitter, requiring specialized test equipment. A numerical example is included in appendix I.

Specifying Jitter Performance

Good jitter performance and low cost are not mutually exclusive as long as:

- The system requirements for jitter are defined in terms of amplitude and spectrum.
- The method used to generate the clock output frequency is optimal for the application.

System Requirements:

Although it is impossible to address all possible variations, some general recommendations based on years of oscillator manufacturing may be helpful.

While not a complete survey of all applications, Table 1 is a starting point for specifying oscillator performance. Jitter above 1 kHz is considered high frequency jitter.

Application Performance Requirements

System Application	Degree of difficulty	Low Frequency Jitter Importance	High Frequency Jitter Importance	Possible Type see table 2
Radar	Very difficult Noise Application	Critical	Critical	A,B,C,D
Ultrasound/MRI	Very difficult Noise Application	Critical	Critical	A,B,C,D
Navigation/GPS	Difficult Noise Application	Critical	High	A,B,C,D
Transmission Systems (telecom)				
Public Network	Moderate Noise Application	Moderate	Moderate	A,B,C,D
Private Network (LAN)	Generally Easiest Application	Low	Low	A,B,F
Frequency Synthesis (see note 1)				
Low Freq. Reference		Moderate-Critical	Moderate-Low	A,B,C
High Frequency Source		Moderate-Low	Moderate-Critical	D,E,F

Note 1: Overall jitter performance is highly dependent on loop parameters.

Table 1

Clock Generation:

Various methods may be employed to generate high frequency clocks.

Performance may vary significantly based on the technique used. Below 20 MHz, it can be assumed that direct crystal frequency generation is sufficient for all but the most critical requirements. Low Noise options should be considered for low jitter applications for 20 MHz and above. Table 2 may be used as a starting point to select a cost-effective solution. Variations and combinations of methods listed in table 2 could also be optimal solutions.

Jitter Performance

Technique	Cost	LF Jitter	HF Jitter	Comments	Type
	1 is lowest	1 is best	1 is best		
	3 is highest	3 is worst	3 is worst		
Direct Clock/TCXO	1	2	1 or 2	Very Good Jitter	A
Direct VCXO	2	1	1 or 2	Very Good Jitter	B
Direct Oven	3	1	1	Excellent jitter	C
Tuned Multiplication	2	1	1 or 2	Periodic Jitter	D
Discrete PLL	2	2	2 or 3	Good Jitter	E
Monolithic PLL	1	3	2 or 3	Close in jitter is poor	F

Table 2

CONCLUSION

To correctly specify performance of frequency sources both jitter frequency and amplitude should be considered. This requires an understanding of jitter, measurement techniques and their limitations. Time spent to determine system needs will result in fewer problems and less time spent fixing those problems later on. It will also determine a cost-effective approach for each application.

In this paper, we discussed the definition of jitter, the units used to describe it, and why jitter is an important parameter. We also reviewed techniques used to measure jitter as well as applications and typical performance based of various kinds of oscillators. The discussion is by no means complete, but should give the reader enough information to understand the issues involved. Industry standards were listed, as well as references for further reading. It is hoped that this paper is useful and considered a good starting point for understanding and specifying jitter.

Appendix A

Integration of Phase Noise to Derive an Equivalent Jitter Number

Equivalent Jitter over various bandwidths may be calculated from the phase noise plot of a clock source. A numerical example using Mathcad7 follows:

Phase noise plots similar to that shown in figure A1 are better understood and analyzed when broken down to their basic components. These components are classified according to their slope as a function of frequency offset. The noise/frequency slopes range from -40 dB per decade ($1/F^4$) to -10 dB per decade ($1/F$) and uniform F^0 slopes. See reference [8] for a more complete treatment of this subject.

From table A1 and phase noise plot A1, break the phase noise components down to areas of major slopes, for instance, the frequency range of $1/F$, $1/F^2$, $1/F^3$ Integrate over the frequency range of interest for each slope (for example, 10 kHz to 10 MHz, or 100 Hz to 10 kHz). Add the results of each integration. The quantity derived from the integration will be an equivalent sideband at the maximum frequency of integration. Treating the calculated sideband as phase modulation allows the calculation of phase deviation. The calculated phase deviation is the equivalent jitter derived from the phase noise plot. Changing the limits of integration will give a better understanding of the effects of jitter at various frequencies. In a like manner, jitter due to subharmonic multiplication may be derived from the subharmonic sideband levels. Note that for each case, the constant of integration is the equivalent noise referred back to zero Hz.

$n := 0..6$ $m := 0..6$

$$\text{data} := \begin{bmatrix} 10^1 & -51 \\ 10^2 & -82 \\ 10^3 & -109 \\ 10^4 & -129 \\ 10^5 & -131 \\ 10^6 & -131 \\ 10^7 & -132 \end{bmatrix}$$

column 0 represents the frequency offset
 column 1 represents the noise below the carrier
 in dB at the corresponding column 0 offset

assume 0 dbm oscillator output level which = 1 milliwatt

$$fdata_n := data_{n,0}$$

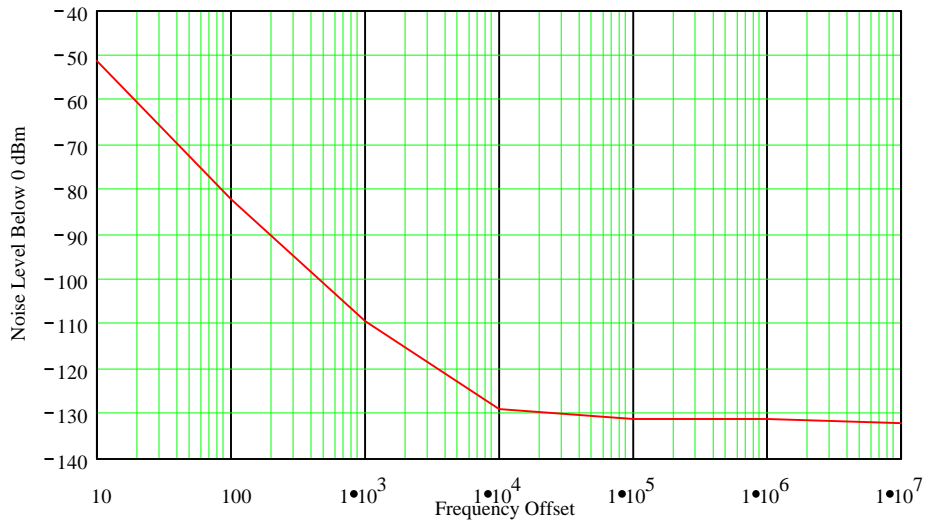
$$pdata_n := 10^{\frac{(data_{n,1})}{10}} \cdot .001$$

$$fdata = \begin{bmatrix} 10 \\ 100 \\ 1 \cdot 10^3 \\ 1 \cdot 10^4 \\ 1 \cdot 10^5 \\ 1 \cdot 10^6 \\ 1 \cdot 10^7 \end{bmatrix}$$

$$pdata = \begin{bmatrix} 7.943 \cdot 10^{-9} \\ 6.310 \cdot 10^{-12} \\ 1.259 \cdot 10^{-14} \\ 1.259 \cdot 10^{-16} \\ 7.943 \cdot 10^{-17} \\ 7.943 \cdot 10^{-17} \\ 6.310 \cdot 10^{-17} \end{bmatrix}$$

offset frequency in Hz

noise power in watts



PLOT A1 Oscillator Phase Noise

$$P1 := \text{pdata}_0 \cdot 10^3 \cdot \int_{10}^{10^2} \frac{1}{f^3} df$$

$$P1 = 3.936 \cdot 10^{-8}$$

Integrate from 10 Hz to 100 Hz

$$P2 := \text{pdata}_1 \cdot (10^2)^3 \cdot \int_{10^2}^{10^3} \frac{1}{(f)^3} df$$

$$P2 = 3.126 \cdot 10^{-10}$$

Integrate from 100 Hz to kHz

$$P3 := \text{pdata}_3 \cdot (10^3)^2 \cdot \int_{10^3}^{10^4} \frac{1}{f^2} df$$

$$P3 = 1.133 \cdot 10^{-13}$$

Integrate from 1 KHz to 10 KHz

$$P4 := \text{pdata}_4 \cdot 1 \cdot \int_{10^4}^{10^7} \frac{1}{F^0} df$$

$$P4 = 7.935 \cdot 10^{-10}$$

Integrate from 10 KHz to 10 MHz

$$Pt := P1 + P2 + P3 + P4$$

Pt = the summation of all integrals

$$Pt = 4.046 \cdot 10^{-8}$$

$$\text{dB} := 10 \cdot \log \left(\frac{Pt}{.001} \right)$$

In this case, the output level reference is 0 dBm (1 milliwatt)

$$\text{dB} = -43.929$$

Equivalent sideband level of integrated phase noise

$$J_{\text{rms}} := \frac{360}{2 \cdot \pi} \cdot 10^{\frac{\text{dB}}{20}}$$

RMS jitter treated as small index phase modulation

$$J_{\text{rms}} = 0.364$$

Equivalent RMS jitter in degrees within the limits of integration

$$\frac{J_{\text{rms}}}{360} = 1.012 \cdot 10^{-3}$$

RMS Jitter given in Unit intervals

$$\frac{J_{\text{rms}}}{360} \cdot \frac{1}{155.52 \cdot 10^6} = 6.51 \cdot 10^{-12}$$

RMS jitter in seconds for a 155.52 MHz signal

Appendix B. References

- [1] John Bellamy, Digital Telephony, Wiley-Interscience, New York, 1991
- [2] Bellcore Communications Research, Clocks for the Synchronized Network: Common Generic Criteria GR-1244-CORE, Piscataway, N.J., 1995
- [3] International Telecommunication Union, <http://www.itu.int/publications>
- [4] Patrick R. Trischitta and Eve L. Varma, Jitter in Digital Transmission Systems Artech House Inc, New York, 1989
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- [7] D.H Wolaver, Phase-Locked Loop Circuit Design, Prentice-Hall, Englewood-Cliffs, NJ, 1991
- [8] D.B. Leeson, "A simple model of feedback oscillator noise spectrum" Proceedings of IEEE, vol. 54, pp. 329-330, February 1996